CLAIMS:

1. A method of forming an electrical connection with a transistor source/drain region of an SOI transistor comprising:

forming a plurality of spaced apart semiconductive material islands over an insulative material, individual islands comprising respective outer surfaces;

forming a conductive transistor gate over at least some of the outer surfaces;

forming at least one conductive source/drain diffusion region within semiconductive material laterally adjacent at least one of the gates;

forming a first conductive material between at least some of the islands and laterally spaced from the one source/drain diffusion region, the first conductive material extending elevationally below the outer surface over which the one conductive gate is formed; and

forming a second conductive material over and in electrical connection with the first conductive material and the one source/drain diffusion region to provide an electrical connection.

2. The method of forming an electrical connection with a transistor source/drain region of claim 1, wherein the forming a first conductive material comprises:

etching insulating material between adjacent islands; and

replacing at least some of the etched insulating material with the first conductive material.

3. The method of forming an electrical connection with a transistor source/drain region of claim 1, wherein:

the islands define respective separation spaces between adjacent islands, at least some of the separation spaces being occupied with insulating material; and

the forming of the first conductive material comprises:

removing at least some of the insulating material occupying at least one of the separation spaces; and

replacing at least some of the removed insulating material with first conductive material to a degree sufficient to only partially occupy the one separation space with first conductive material.

4. The method of forming an electrical connection with a transistor source/drain region of claim 1, wherein:

individual islands have respective sidewalls and define respective separation spaces between adjacent island sidewalls, at least some of the separation spaces between island sidewalls being occupied with insulating material; and

the forming of the first conductive material comprises:

etching at least some of the insulating material occupying at least one of the separation spaces to a degree sufficient to expose at least a portion of an island sidewall;

forming additional insulating material over the exposed island sidewall portion and to a degree sufficient to leave at least a portion of the separation space unoccupied with any additional insulating material; and

forming first conductive material within the remaining unoccupied separation space.

5. A method of forming an electrical connection comprising:

forming a diffusion region in semiconductive material, the diffusion region having an outer surface;

forming a conductive line laterally spaced from the semiconductive material and diffusion region, a predominate portion of the conductive line being disposed elevationally below the diffusion region outer surface; and

interconnecting the conductive line and the diffusion region with electrically conductive material.

6. The method of claim 5, wherein ~~the~~ interconnecting the conductive line and the diffusion region comprises forming the electrically conductive material over both the conductive line and the diffusion region.

7. The method of claim 5, wherein the forming of the conductive line comprises:

forming an isolation oxide region laterally adjacent the semiconductive material, the oxide region having a lateral width;

removing a portion of the isolation oxide intermediate the lateral width; and

replacing at least some of the removed isolation oxide with electrically conductive material.

8. The method of claim 5, wherein the forming of the conductive line comprises:

forming an isolation oxide region laterally adjacent the semiconductive material, the oxide region having a lateral width;

removing a portion of the isolation oxide intermediate the lateral width and to a greater degree in an elevationally downward direction than a laterally outward direction; and

replacing at least some of the removed isolation oxide with electrically conductive material.

9. The method of claim 5, wherein the forming of the conductive line comprises:

forming an isolation oxide region laterally adjacent the semiconductive material, the oxide region having a first lateral width;

removing a portion of the isolation oxide at least intermediate the lateral width;

forming oxide material within the first lateral width and to a degree sufficient to occupy less than the first lateral width and to define a second lateral width; and

replacing at least some of the removed isolation oxide with electrically conductive material.

10. A method of forming at least one interconnection to a node location in SOI integrated circuitry comprising:

forming a conductive diffused node location in a silicon-containing structure, the structure being formed over and surrounded by isolation oxide;

forming a first conductive material laterally adjacent the silicon-containing structure, a predominate portion of the first conductive material being disposed elevationally below the diffused node location; and

forming a second conductive material over at least a portion of the first conductive material and the node location to provide an electrical interconnection therebetween.

11. The method of claim 10, wherein the first conductive material and the second conductive material comprise the same material.

12. The method of claim 10, wherein the first conductive material and the second conductive material comprise the different materials.

13. The method of claim 10, wherein the forming a first conductive material comprises:

etching the isolation oxide and exposing at least a portion of the silicon-containing structure, the etching defining an elongated trench for receiving first conductive material; and

filling at least a portion of the trench with first conductive material.

14. The method of claim 10, wherein the forming a first conductive material comprises:

etching the isolation oxide and exposing at least a portion of the silicon-containing structure, the etching defining an elongated trench for receiving first conductive material;

depositing an oxide material within the trench and over the exposed portion of the silicon-containing structure, the oxide material defining a trough within the trench; and

filling at least a portion of the trough with first conductive material.

15. The method of claim 10, wherein the forming a first conductive material comprises:

etching the isolation oxide to a degree sufficient to expose a silicon-containing sidewall of the silicon-containing structure and a silicon-containing sidewall of another laterally adjacent silicon-containing structure, the two silicon-containing sidewalls generally facing one another and defining a trench therebetween;

forming an oxide lining within the trench and over the two silicon-containing sidewalls, the oxide lining defining a trough within the trench; and

forming first conductive material within at least a portion of the trough and over at least some of the oxide lining.

16. A method of forming integrated circuitry comprising:

forming a diffusion region within semiconductive material between spaced apart isolation oxide regions;

forming a conductive line within at least one of the isolation oxide regions adjacent the diffusion region; and

forming conductive material over the diffusion region and the conductive line to provide an electrical interconnection therebetween.

17. The method of forming integrated circuitry of claim 16, wherein the forming a conductive line comprises:

etching the one isolation oxide region to elevationally below the diffusion region; and

forming conductive line material within the one isolation region.

18. The method of forming integrated circuitry of claim 16, wherein the forming a conductive line comprises:

etching the one isolation oxide region to elevationally below the diffusion region, the etching defining a lateral width dimension in a width dimension direction;

forming oxide material within the lateral width dimension and to a degree sufficient to occupy about two thirds of at least some of the lateral width dimension in the width dimension direction; and

forming conductive line material in at least some of the lateral width dimension which is not occupied with oxide material.

19. A method of forming an electrical connection to a node location comprising:

forming at least one isolation trench within a bulk semiconductive substrate, the isolation trench being disposed laterally adjacent a substrate active area;

filling the one isolation trench with isolation oxide;

removing some of the isolation oxide from the one isolation trench;

replacing the removed isolation oxide with first conductive material;

forming a diffusion region in the substrate active area, the diffusion region defining a node location to which electrical connection is to be made; and

forming second conductive material over the first conductive material and the diffusion region to provide an electrical connection therebetween.

20. The method of forming an electrical connection to a node location of claim 19, wherein the diffusion region has an outer surface and the first conductive material is formed to extend predominately below the diffusion region outer surface.

21. The method of forming an electrical connection to a node location of claim 19 further comprising forming at least one conductive gate within the active area.

22. The method of forming an electrical connection to a node location of claim 19, wherein:

the forming of the one isolation trench comprises forming at least two isolation trenches which are laterally spaced from one another, the trenches being thereafter filled with isolation oxide; and

the removing comprises removing only some isolation oxide from both trenches, the removed isolation oxide being thereafter replaced with first conductive material.

23. The method of forming an electrical connection to a node location of claim 19, wherein the first conductive material and the second conductive material comprise the same material.

24. The method of forming an electrical connection to a node location of claim 19, wherein the first conductive material and the second conductive material comprise different materials.

25. A method of forming conductive lines comprising:

forming an oxide isolation grid between semiconductive material;

forming conductive material within the oxide isolation grid to form a conductive grid therein; and

removing selected portions of the conductive material grid to define interconnect lines within the oxide isolation grid.

26. The method of forming conductive lines of claim 25, wherein the forming an oxide isolation grid comprises forming individual oxide isolation regions over a semiconductive substrate by trench and refill technique.

27. The method of forming conductive lines of claim 25, wherein the forming an oxide isolation grid comprises:

forming a plurality of silicon-containing islands over an insulative surface; and

forming oxide isolation regions between silicon-containing islands.

28. The method of forming conductive lines of claim 25, wherein the forming conductive material within the oxide isolation grid comprises:

etching into the oxide isolation grid to define a network of outwardly-exposed trenches running within the oxide isolation grid;

forming conductive material within and over the outwardly-exposed trenches to a degree sufficient to completely fill the trenches; and

planarizing the conductive material to isolate conductive material within the trenches and to define the conductive grid.

29. A method of forming a conductive grid over a substrate comprising:

forming a layer of insulative material over a substrate surface;

forming a plurality of upstanding silicon-containing structures over the insulative material, the silicon-containing structures comprising respective outer surfaces;

defining a network of conduits within the insulative material between individual silicon-containing structures; and

filling the conduits at least partially with conductive material to provide a conductive grid.

30. The method of forming a conductive grid of claim 29, wherein defining a network of conduits comprises etching at least some of the insulative material between individual silicon-containing structures to below an adjacent silicon-containing outer surface.

31. The method of forming a conductive grid of claim 29, wherein:

the defining a network of conduits comprises etching at least some of the insulative material between individual silicon-containing structures to a degree sufficient to expose respective silicon-containing structure sidewalls; and

prior to filling the conduits at least partially with conductive material, forming an oxide lining material within the conduits and over the exposed respective silicon-containing structure sidewalls.

32. A method of forming a conductive network comprising:

forming a plurality of oxide isolation regions over a semiconductive substrate; and

forming conductive material received within at least one of the oxide isolation regions.

33. The method of forming a conductive network of claim 32, wherein the forming a conductive material comprises:

etching into at least some oxide isolation region material;

forming conductive material within the etched oxide isolation regions; and

planarizing the conductive material to a degree sufficient to isolate desired conductive material relative to other conductive material, the planarizing defining the conductive network.

34. The method of forming a conductive network of claim 32, wherein the forming a conductive material comprises:

etching into at least some oxide isolation region material;

chemical vapor depositing an oxide lining material within the etched isolation regions;

forming conductive material within the etched oxide isolation regions and over oxide lining material; and

planarizing the conductive material to a degree sufficient to isolate desired conductive material relative to other conductive material, the planarizing defining the conductive network.

35. The method of forming a conductive network of claim 32, wherein the forming a conductive material comprises:

etching into at least some oxide isolation region material;

chemical vapor depositing an oxide lining material within the etched isolation regions;

forming conductive material within the etched oxide isolation regions and over oxide lining material;

planarizing the conductive material to a degree sufficient to isolate desired conductive material relative to other conductive material, the planarizing defining the conductive network; and

removing selected conductive material to define a plurality of interconnect lines.

36. A method of forming conductive lines in electrical contact with active area diffusion regions comprising:

forming insulative material over a semiconductive substrate;

forming a plurality of silicon-containing structures over the insulative material, individual silicon-containing structures having respective sidewalls, adjacent silicon-containing structure sidewalls defining respective spaces therebetween;

forming nitride-containing caps atop the individual silicon-containing structures;

forming insulative material in the spaces between individual adjacent silicon-containing structures;

planarizing the insulative material to be generally coplanar with the nitride-containing caps;

etching at least some of the insulative material between individual adjacent silicon-containing structures to a degree sufficient to expose the respective sidewalls of the adjacent silicon-containing structures, the etching defining respective troughs between the sidewalls having lateral widths in lateral width directions;

depositing an oxide lining material within the troughs and over respective sidewalls to a degree sufficient to fill about two thirds of the lateral width of the trough in the lateral width direction;

forming conductive material over the substrate and in at least some of the remaining one third of the lateral width of the trough;

planarizing the oxide lining material and the conductive material to be substantially coplanar with nitride-containing caps;

recessing remaining conductive material within the trough to below an immediately adjacent planar surface;

masking selected substrate areas;

removing conductive material from unmasked substrate areas;

forming insulative material over the substrate, the insulative material filling in the troughs from which conductive material was removed and covering conductive material which was not removed;

planarizing the insulative material to be substantially coplanar with the nitride-containing caps;

removing the nitride-containing caps to outwardly expose respective outer surfaces of the silicon-containing structures, respective outer surfaces defining individual active areas in which diffusion regions are to be formed;

forming individual oxide layers over respective silicon-containing structure outer surfaces;

forming a polysilicon layer over the oxide layers;

planarizing the polysilicon layer;

forming an oxide layer over the polysilicon layer to provide stack structures over the silicon-containing structures;

patterning and etching the stack structures to form individual gate structures over the silicon-containing structures;

forming sidewall spacers over respective gate structure sidewalls;

forming diffusion regions in the silicon-containing structures adjacent individual gate structures;

forming insulative material over the substrate;

planarizing the insulative material;

patterning and etching the insulative material to outwardly expose at least one diffusion region and at least some of the conductive material; and

forming connective polysilicon material over the one exposed diffusion region and the conductive material, the connective material interconnecting the one exposed diffusion region and the conductive material, the conductive material providing a conductive line to the one diffusion region.

37. Integrated memory circuitry comprising:

a substrate;

a plurality of source/drain diffusion regions supported by the substrate;

a plurality of isolation oxide regions supported by the substrate and interposed between and separating at least some of the source/drain diffusion regions; and

a plurality of conductive lines supported by the substrate at least some of which being operatively connected with at least some of the source/drain diffusion regions and disposed within the isolation oxide regions.

38. The integrated memory circuitry of claim 37 further comprising a plurality of silicon-containing structures, the structures being separated by respective isolation oxide regions and supporting respective source/drain diffusion regions.

39. The integrated memory circuitry of claim 37, wherein the source/drain diffusion regions define respective outer surfaces and a predominant portion of at least some of the conductive lines which are disposed within the isolation oxide regions are disposed elevationally below the source/drain diffusion regions' outer surfaces.